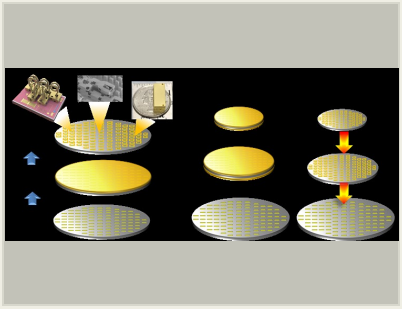
Wafer level Integration on PolyStrata(R) Interposer (WIPI) (17013), Phase I

Completed Technology Project (2017 - 2017)

Project Introduction

Nuvotronics will develop a robust wafer-level integration technology using our proprietary PolyStrata interposer to enable high-frequency interconnects and routing between two dis-similar substrates: silicon, SiGe, GaAs, GaN, InP wafers. The PolyStrata passives grown on the wafers will consist of high performance interconnects capable of aligning and soldering the two wafers using copper pillars to create a Ball Grid Array (BGA). Establishing novel wafer-to-wafer push fit technologies will demonstrate sub 5psec interconnection delay between technologies. With integration of low loss routing between the technologies, our proposed interposer can monolithically integrate passives such as high Q inductors, filters, resonators directly between the two wafers. The PS interposer offers an excellent structure to improve the CTE mismatch between wafers and enable thermal heat piping to direct the heat away from the different stack. In Ph I, Nuvotronics will demonstrate the integration of GaAs on Silicon using the PS interposer technology. The goal: to integrate a 1"x1" GaAs and Silicon die, demonstrating interface loss < 0.3dB and sub 5psec interconnection delay. The design will integrate CTE compensation structure to enable over 100C of temperature variation. Nuvotronics will design and optimize the interface between PolyStrata and silicon, and between GaAs and PolyStrata, to minimize stress and improve mm-wave RF performance. Next, Nuvotronics will fabricate a surrogate silicon and surrogate GaAs wafer with PolyStrata interface. A solder ball back-end process will be applied to both wafer technology and integration of solder balls. The 4" wafers will be diced in 1"x1" dies before being integrated. DC and RF measurements will demonstrate electrical performance. Preliminary temp. cycling will be performed to demonstrate reliability of the interface. In Ph II, Nuvotronics will demonstrate 4-inch wafer level integration and performance under temp. cycling.



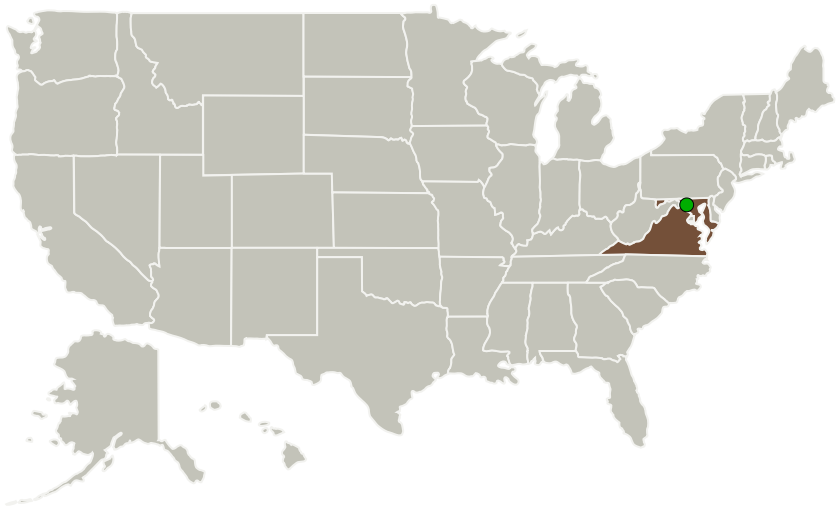
Wafer level Integration on PolyStrata(R) Interposer (WIPI) (17013), Phase I Briefing Chart Image

Table of Contents

Wafer level Integration on PolyStrata(R) Interposer (WIPI) (17013), Phase I

Completed Technology Project (2017 - 2017)

Primary U.S. Work Locations and Key Partners



Organizations Performing Work	Role	Type	Location
Nuvotronics, Inc	Lead Organization	Industry	Radford, Virginia
Goddard Space Flight Center(GSFC)	Supporting Organization	NASA Center	Greenbelt, Maryland

Primary U.S. Work Locations	
Maryland	Virginia

Organizational Responsibility

Responsible Mission Directorate:

Space Technology Mission Directorate (STMD)

Lead Organization:

Nuvotronics, Inc

Responsible Program:

Small Business Innovation Research/Small Business Tech Transfer

Project Management

Program Director:

Jason L Kessler

Program Manager:

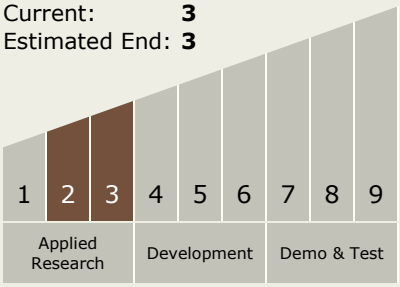
Carlos Torrez

Principal Investigator:

Scott A Meller

Technology Maturity (TRL)

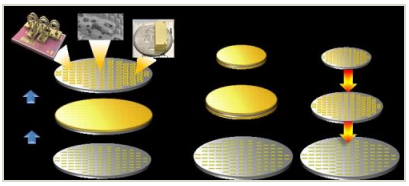
Start: **2**
Current: **3**
Estimated End: **3**



Wafer level Integration on PolyStrata(R) Interposer (WIPI) (17013), Phase I

Completed Technology Project (2017 - 2017)

Images



Briefing Chart Image
Wafer level Integration on PolyStrata(R) Interposer (WIPI) (17013), Phase I Briefing Chart Image
(https://techport.nasa.gov/image/135763)

Technology Areas

Primary:

- TX08 Sensors and Instruments
  - TX08.1 Remote Sensing Instruments/Sensors
    - TX08.1.4 Microwave, Millimeter-, and Submillimeter-Waves

Target Destinations

The Sun, Earth, The Moon, Mars, Others Inside the Solar System, Outside the Solar System